Electronics Milestones and Planning

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Summarize progress and propose milestones for FE, MCC, and Opto-link electronics schedules

Warning: major electronics meetings of this ATLAS week have not yet taken place, so this discussion should be regarded as preliminary

Major Near-term Goals for On-Detector Electronics

Front-end Chips:

- Complete demonstrator effort by submitting demonstrator designs in the two candidate radhard processes
- TEMIC/DMILL version to be completed first (so-called FE-D)
- Honeywell/HSOI version to follow as soon as possible (so-called FE-H)

Module Controller Chip:

- Begin prototyping in radhard processes, submitting test chips with standard cells and large blocks (FIFO, I/O drivers, DACs and delays...)
- Radhard MCC will not be implemented for demonstrator generation. Next step is to work on “Phase II” system design, to be followed later by actual chip. Likely to pursue only one of two radhard vendors for this chip due to limited manpower.

Opto-link Electronics:

- Begin using prototype SCT chips (DORIC4, VDC, BPM, DRX)
- Explore either radhard CMOS versions or radhard bipolar versions of DORIC4 and VDC
- Begin working with GEC opto-package and explore pixel-specific options and second source options.

Opto-link Electronics

Recent progress:

- Last week, we had a several day meeting in Oxford with SCT opto-link experts to discuss various aspects of their design.
- We reviewed the opto-electronics chips (DORIC4, VDC, BPM, DRX) with the chip designers, as well as the existing system test results
- We discussed the present GEC package in detail and discussed pixel-specific issues. We also discussed the ROD optoboard and the optical components on the off-detector end
- We reviewed the SCT system design, both on and off detector, and explored pixel/SCT differences
- Michal will summarize some of these issues at the Nov 17 Electronics meeting.

Short-term plan:

- We arrived at a short-term plan for the opto-link effort for pixels

Chip Designs:

- This plan includes a collaborative effort by OSU and Siegen to evaluate the existing DORIC and VDC designs, and explore their implementation in radhard CMOS.
- This would give us a low power and general solution for circuits that could be included in the MCC. This activity should show significant progress by the Feb ATLAS week.
- If this approach looks as though it would compromise the performance significantly, or is not appropriate, then the effort would switch to a radhard bipolar implementation in DMILL, which could be a stand-alone chip, or a part of a DMILL MCC.

Optolinks and board electronics:

- We discussed a first phase of system tests to take place during 99.
- One aspect would be characterizing and implementing the prototype opto-link packages from GEC onto a module in 99.
- The second aspect would be designing an opto-board appropriate for use with our existing PLL system for operation of a single module with an optical interface.
- These aspects would be handled jointly by OSU (and Wuppertal ?) and Siegen, with OSU concentrating on the first, and Siegen concentrating on the second.

- This activity should focus on being prepared to move ahead quickly with GEC packages when they arrive in Summer 99. It should result in useful tests of the system by Fall 99.
- In parallel, the SCT community will move ahead with the full ROD opto-board (an Oxford/Cambridge collaboration) and a test in the multi-module context. We will follow this work, but not participate directly.

Module Controller Chip

Prototyping Work:

- First step will be to implement layout of some critical blocks, such as the large input FIFO, in DMILL for a Feb 99 MPW run. This work will start in Dec when Roberto Beccherle spends several weeks at LBL working with Gerrit Meddler.
- This run would also include some other blocks, and might include a radhard MCC replacement chip which could be used in the short-term to make radhard modules.
- Similar work would probably be pursued for Honeywell SOI to allow a realistic comparison of the size and performance of the two versions of the MCC. The HSOI process, particularly for standard cell design where the extra metal layers (there are 4 in HSOI and 2 in DMILL) can give significant added routing ability, could have real advantages.
- Additional functions (presently in PCC) that are not in demonstrator MCC need to be designed and prototyped. Some examples would include the VCal DAC and the Strobe delay generator. Further elements would be defined as part of “Phase II” system design.

Work on rad-hard MCC:

- Still significant remaining work needed on testing existing chip. Genova is building a dedicated VME-based test module to allow input of arbitrary (and even incorrect) simulated data streams from 16 FE chips, etc.
- Begin process of defining “Phase II” system design discussions this week. Expect this will be a continuing discussion within a working group for 4-6 months. It should lead to new specification documents, similar to those produced for the demonstrator effort.
- Actual design effort for the MCC not yet organized. Would expect this to begin in mid-99, and lead to a chip in early 00. Genova has asked for additional manpower, and it is likely that Bonn and LBL (and perhaps others) will supply additional help on this effort after the present generation of radhard FE chips are completed.

Front-end Chips

Present status:

- After agreement on “common design” effort in June, held a large designer meeting in mid-July. In June, it was already agreed that we would first do a DMILL chip (so-called FE-D), to be followed by a Honeywell SOI chip (so-called FE-H). At the July meeting, we agreed on the scope of the radhard demonstrator work.
- The new designs preserve geometric and electrical compatibility with the existing radsoft chips, to allow mixing of detectors, test boards, etc. Major additions include improved performance in the readout architecture, emphasis on rad-tolerance of designs, and elimination of any known bugs.
- The division of tasks among the three contributing groups (Bonn, CPPM, LBL) was agreed in July for the FE-D chip, and work began.
- Some highlights include:

  Installation of FE-A/FE-B/MAREBO design databases in common CAD area at Bonn.

  First pass at full analog section (pixel front-end and bias circuitry) from CPPM

  First pass at improved readout section (back of pixel and end of column buffering) should come from LBL this week.

  First pass at overall floorplan, and inclusion of many existing blocks at Bonn.

- Overall, the startup of this design effort has been slower than anticipated. This is in large part due to the large amount of other FE electronics activity within the groups (testbeam, irradiations, continued evaluation of existing designs, parallel effort to prepare for Honeywell design, etc.)
- The communication among the people involved needs to be improved, and we will probably institute regular phone meetings to try to develop more efficient and informed collaboration.

Outstanding issues:

- There is the general sense that we are behind schedule on FE-D compared to our original intentions (submission on Jan. 99 timescale was discussed in July).
- There is disagreement over how best to pursue the dual goals of FE-D and FE-H, and what work needs to be done when to achieve these goals.
- There is disagreement about exactly what the FE-H design should include, and what differences from the FE-D submission might be useful, as well as about what tasks will be performed by which groups.
- The so-called “TAA” agreements which allow non-US groups to work with the Honeywell process are moving very slowly. This will delay the ability of Bonn and CPPM to do design work in their home institutes on FE-H.
- There is a request (requirement), from both ATLAS and US ATLAS, that these designs require proper review before submission of the chips.

Proposed FE-D Schedule (realistic):

- Next significant milestone will be the assembly of the large top-level blocks into a complete design. At that time, the major simulation effort on these blocks should have been carried out, and they should be in fairly mature form. This should happen by about the end of Dec.
- At this point in the effort, propose to have a review, organized by the overall FE Electronics coordinator. It would be a 1-2 day review and the team would most likely include 4 designers from the ATLAS community. A plausible date for this (to be ratified by the designers meeting next weekend) is about Jan. 18.
- There would be a second review about 4-6 weeks later, at which time we would expect to have completed the top-level simulations, plus overall LVS and DRC. Assuming no major problems uncovered in Jan., this would be about the time of the Feb. ATLAS week.
- This would lead to a submission date of about the end of March, assuming that it always requires a few weeks after the last review to be really ready. This is somewhat later than we had originally proposed, but I think it is still a very “success-oriented” schedule given our recent progress.
- This would give us chips by about Aug 1, which could still allow evaluation in the Sept H8 testbeam and irradiation in Oct. PS beam period.
- We will know more after the designers meeting...

Organization and priority of FE-H work:

- Our stated goal is to have a FE-H submission which is on a “similar” schedule to the FE-D. This should mean a submission date which is delayed by less than 6 months relative to the FE-D submission, or latest by Sept 1 99. Ideally, the difference in submission dates would be more like 4 months.
- Already, such a schedule prevents us from doing any evaluation of FE-H during 99 and presents significant schedule problems to ATLAS for the evaluation of this chip.
- Meeting this schedule requires significant parallel effort on HSOI prior to the submission of FE-D, particularly in the analog front-end area.
- The present status of the TAA agreements for Bonn and CPPM is that the paperwork is basically ready to be sent to the US Govt. Historically, processing times of about 4 months are typical. This would mean that it might not be possible for Bonn and CPPM to work on HSOI design in their home institutes before some time in March. We are trying to expedite this process, but it is not clear how much influence anyone can have...
- Our present best expert in HSOI (Franz Pengg) is very likely to leave during Jan 99. This will leave us with only one analog designer, and much less SOI expertise in our designer collaboration.

- Finally, the significantly greater capabilities of the HSOI process allow us, in my opinion, to do a much better (i.e. more reliable, including better diagnostics, and most likely better performance) design. This leaves room for real common design effort (the FE-D by comparison is really a merger of pieces of existing designs, with some modest improvements in readout performance). It would be a mistake not to take advantage of this opportunity to make a better FE chip for ATLAS.

Next steps:

- We need to improve our collaboration on the FE-D effort. The manpower situation at LBL should improve somewhat, and we may need to consider some redistribution of tasks to improve our efficiency (transfer from LBL to Bonn).
- We have an opportunity to submit several test circuits in HSOI, in particular, an analog front-end test chip of a common design. We should try hard to do something useful for that run, despite the fact that test chips would not be available before June or so.
- We need to clearly define the tasks for the FE-H submission, and their distribution between institutions, given all of the other constraints.